National Semiconductor

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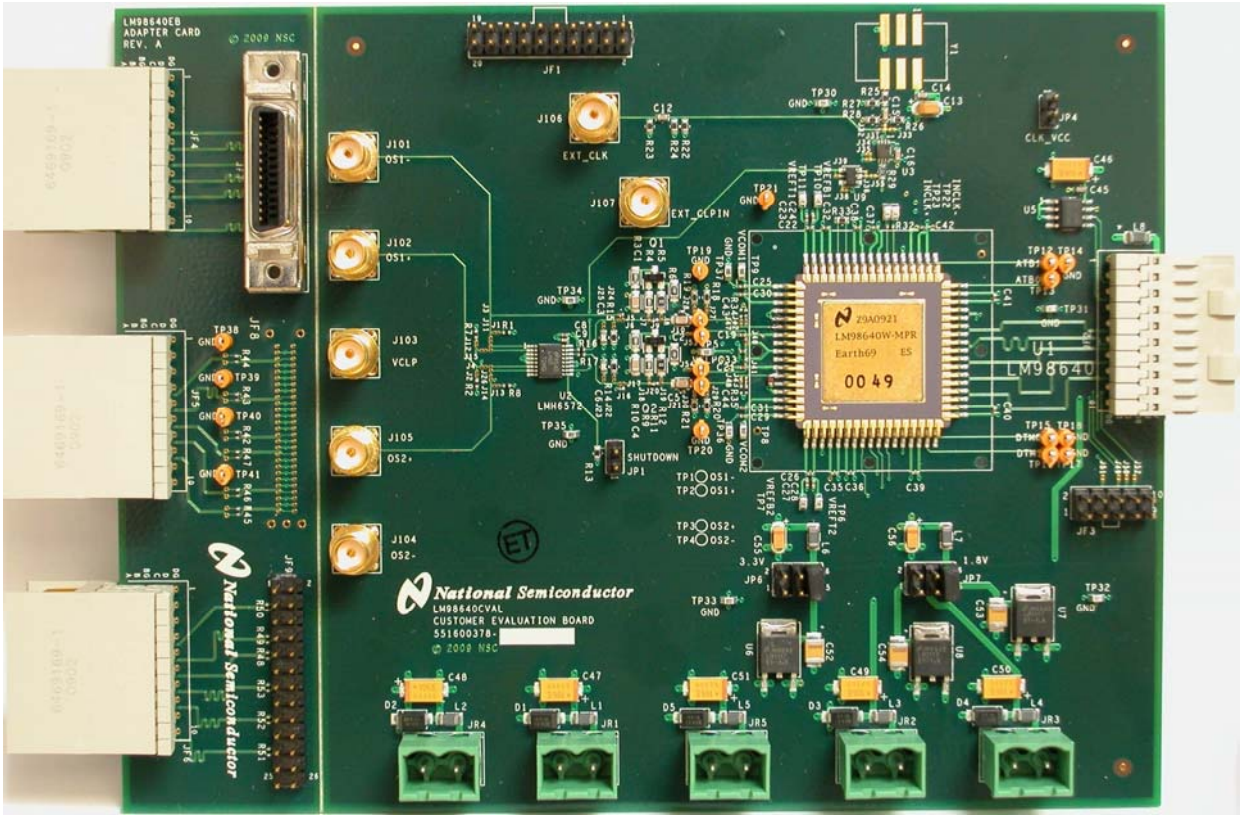
LM98640CVAL Evaluation Board User's Guide

LM98640QML Dual Channel Analog Front End Evaluation Board



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1.0 Introduction

The LM98640CVAL Board is designed to allow quick evaluation and design development of National Semiconductor's LM98640QML Analog Front End. This development board is designed to function in several different configurations.

The primary configuration connects the LM98640QML evaluation board to National Semiconductor's Wavevision 5 Data Capture Board (WV5). The AFEval software is used to communicate to the LM98640QML's SPI port as well as retrieve Data Output from the device for display or external analysis. The present revision of the WV5 board is limited to 30k samples per channel. Future revisions will allow for very deep memory capture (up to 8MB total).

The LM98640QML evaluation board also comes with an auxiliary adapter card. This card allows the LM98640QML output to be routed to one of three connectors for external data capture and analysis. To facilitate this configuration, a Total Phase Aardvark I2C/SPI Host Adapter is supplied to perform the SPI communication using the AFEval tool.

A PCB footprint for and external clock oscillator is provided on board to allow testing without the need of an external clock source. An SMA connection is available for connecting an external clock source when a variable frequency may be desired.

The power supply for the LM98640QML and surrounding circuitry can be made through the WV5 board or from external bench top supplies when the WV5 board is not being implemented.

The CCD signal inputs are made via SMD type connections. The signals can be routed directly to the AFE, AC coupled, emitter follower buffered, or sent into a video multiplexer to create a CCD type signal from a non CCD source.

2.0 Board Assembly

The LM98640CVAL Evaluation Board comes pre-assembled. Refer to the Bill of Materials in *Section 6* for a description of components, to *Figure 1* for major component placement and to *Section 4* for the Evaluation Board schematic. The Evaluation Board comes as a single board with two distinct partitions. The Evaluation partition is on the right side, and the Adapter Card is on the left. The two partitions should be carefully separated to connect the AFE data output to the desired Adapter Card connector.

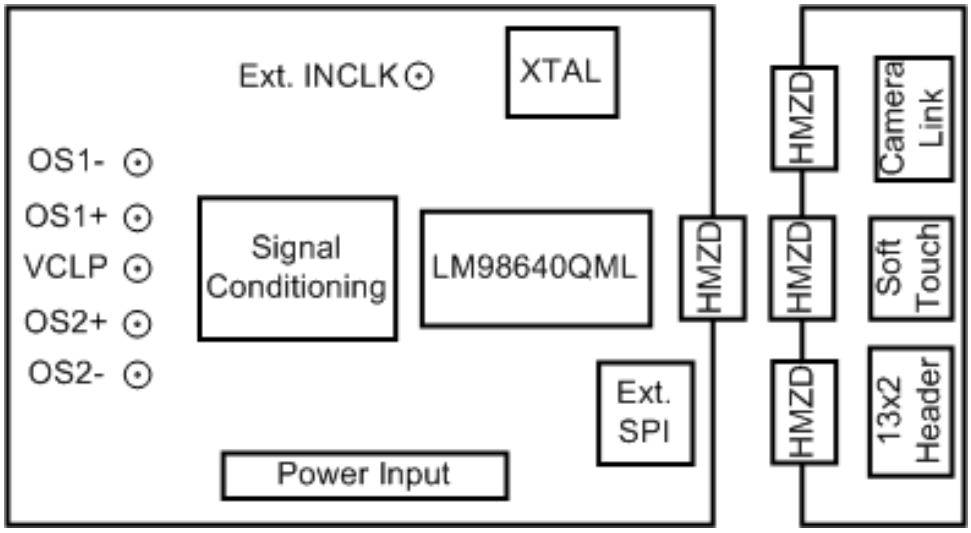


Figure 1. Evaluation Board Layout

3.0 Functional Description

The LM98640CVAL Customer Evaluation Board schematic is shown in Section 4.

3.1 Power Supply Connections

The power supplies on the LM98640CVAL Customer Evaluation Board are configurable to provide several options in powering the AFE and other devices on board. There are two main supplies for the device, +3.3V and +1.8V. The sources for these supplies are selectable by setting jumpers JP6 and JP7.

The default power configuration for the LM98640CVAL Customer Evaluation Board is a single +5V supply connected through the JR1 connector. The +3.3V and +1.8V supplies are generated from this +5V supply using on board regulators.

The user also has the option to use external +3.3V and +1.8V supplies through the JR2 and JR3 connectors.

The third option will allow the external +3.3V supply to be sourced from the data output HMZD connector. This configuration allows the WV5 board to supply power to the LM98640QML without the need for any other external supplies.

Power for the optional analog input emitter followers is derived from the Vext supply only. This allows the emitter follower to be powered up to 18V to allow signals from a CCD Sensor with a high voltage range.

Power for an onboard pseudo CCD signal generator is supplied by the external +5V and -5V connections.

The polarity of the external power supply connections are shown below.

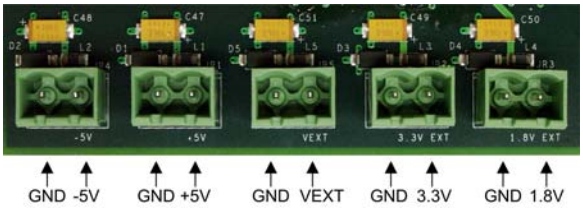


Figure 2. External Power Supply Connections

3.2 AFE Analog Input Section

The Analog signals for the LM98640CVAL Board enter through SMA connectors and there are a variety of options onboard to modify or condition the input signal to meet the specifications of the LM98640QML analog inputs.

Signals can be AC coupled using capacitors C2 and C5, the bias point for the AFE side of the AC coupling capacitor can be set by using the internal CLPIN features of the AFE or by using the onboard resistor divider of R18, R19 and R20, R21.

Signals can also be driven DC coupled and can be 50Ω terminated near the SMA or near the AFE input. Signals can also be filtered using capacitors C43 and C44.

For signal sources that cannot drive a 50Ω load an onboard emitter follower can be used. The emitter follower has a dedicated supply through Vext (JR5) and can be powered up to 18V.

A pseudo CCD signal generator can be used to create a custom CCD signal for test and evaluation purposes. The pseudo CCD signal generator takes two signals and switches between them based on the input clock. These two signals can be set to create a CCD waveform with a fixed reference level and varying video level. The pseudo CCD signal generator is powered from the +5V and -5V supply connectors (JR1 and JR2).

The VCLP voltage signal can be supplied from SMA J103 or generated by the internal VCLP DAC of the AFE. If using the external VCLP the user must ensure the internal VCLP DAC is disabled. The VCLP signal can be externally tied to the OS_X+ pins using jumpers J40 and J41.

To enable or disable any of these circuits the appropriate solder bump jumpers must be opened or closed. Refer to the Analog Input schematic on sheet 2.

3.3 AFE Input Clock Circuit

The clock for the LM98640QML can be supplied by one of three methods. External clocks can be provided at either the JF1, 20 pin dual row header on pin 1, or the J106 SMA connector. An on board crystal oscillator (Y1) is configured as the primary source. Changing the clock source from the on board oscillator to one of the external sources involves reconfiguring the solder bump jumpers shown on schematic page 4.

Clock Source	Jumper Configuration		
	J32	J31	J33
On Board Crystal Oscillator Y1	short	open	open
External Clock at JF1 Dual Row Header	open	open	short
External clock on J106 SMA Connector	open	short	Open

3.4 AFE Data Output

The LM98640QML LVDS output signals are run to an HMZD connector (JF2). The Wavevision 5 Data Capture Board mates directly to this connector.

IMPORTANT: The Wavevision 5 Data Capture board is loaded with an FPGA image to deserialize the LM98640QML data outputs. At the time of this publishing, the FPGA image supports Quad Lane output mode through the entire operating range (i.e. 5MHz to 40MHz). Dual Lane Mode will function from 5MHz to 35MHz. If the LM98640QML is configured in Dual Lane Mode and the frequency is greater than 35MHz, unexpected results may occur.

To facilitate other methods of evaluation, the LM98640CVAL Customer Evaluation boards come with a daughter board that has three types of connectors: a 3M MDR Camera Link connector, an Agilent Soft Touch connector, and an 18 pin dual row header. To select a particular connector the associated HMZD connector should be connected to the HMZD connector of the main AFE board.

Each connector of the daughter board has termination resistors at the connector. These resistors can be lifted from the board if the end receiver has its own termination resistors.

3.5 AFE Serial Interface

The LM98640QML uses a 4-wire Serial Interface to read/write the configuration registers. The Customer Evaluation Board provides a 2x5 pin header (JF3) to directly interface to the AFE Serial Interface.

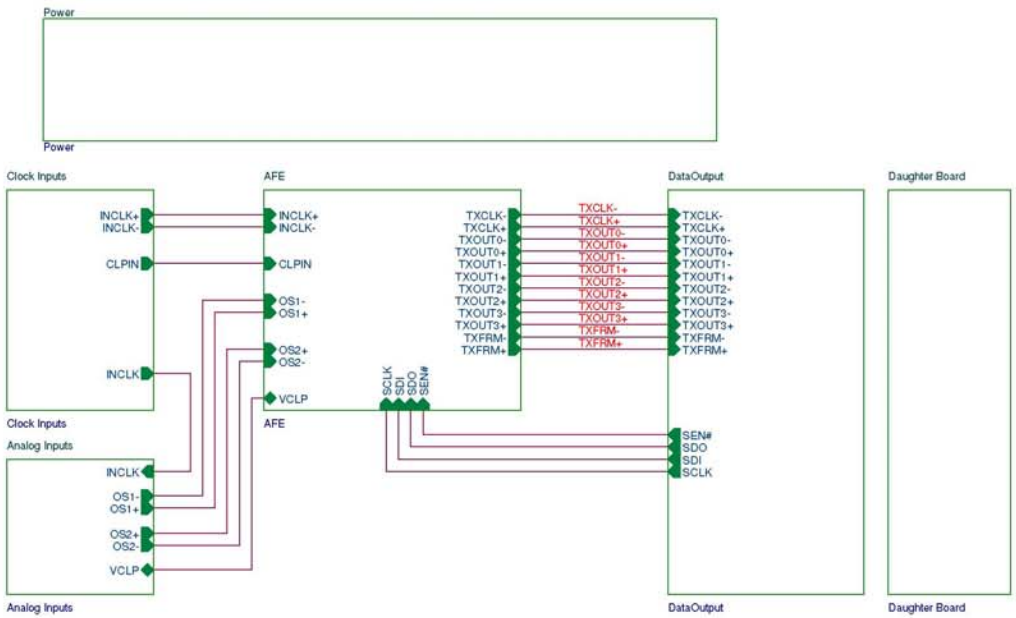
When the Wavevision 5 Data Capture board is connected, the serial communication will be automatic. The J49, J50, J51, and J52 solder jumpers must be connected to enable the WV5 communication.

In the case where the WV5 board is not being used, the Total Phase Aardvark I2C/SPI Host Adapter can provide the SPI communication. This device connects to the 2x5 pin dual row header and a USB connection to a PC.

In either instance (WV5 or Aardvark), the AFEval software provides the GUI interface for the communication. See Appendix A and B for more information on the Register Configuration Software.

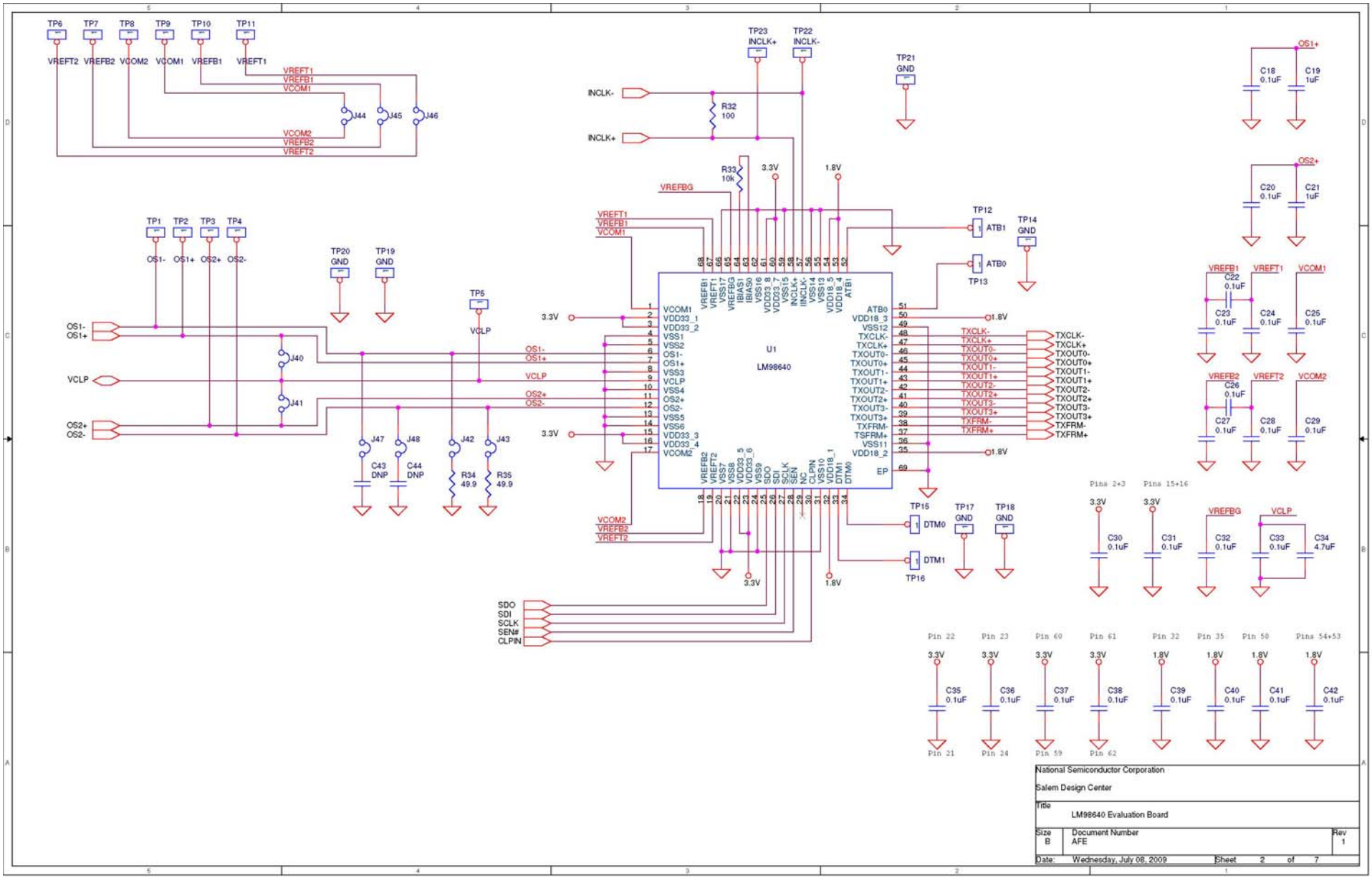
4.0 Schematic Drawing LM98640QML

4.1 Page 1: Top Level Block Connectivity

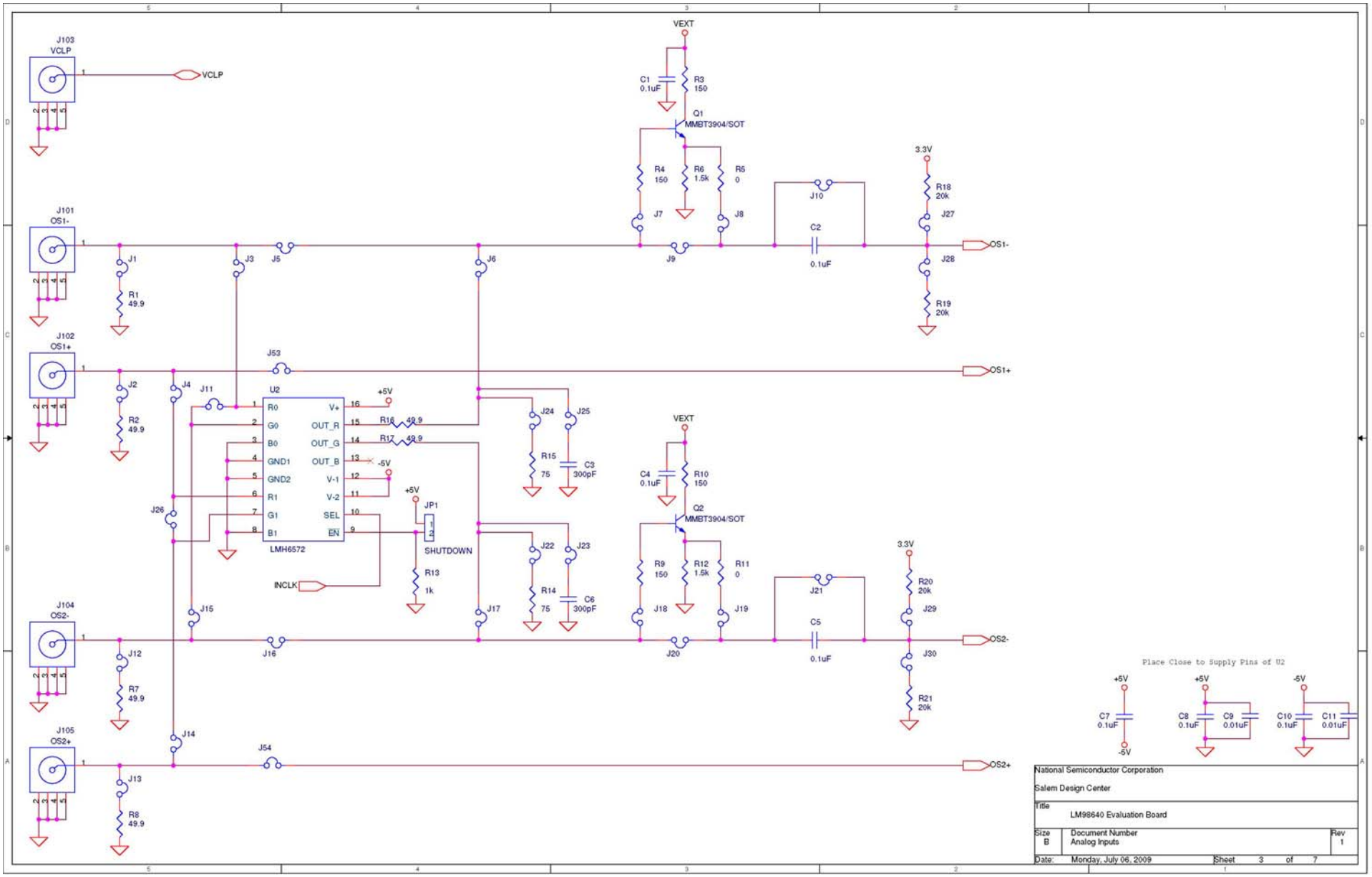


National Semiconductor Corporation Salem Design Center		
Title LM98640 Evaluation Board		
Size B	Document Number TOP	Rev 1
Date: Monday, July 06, 2009	Sheet 1 of 7	

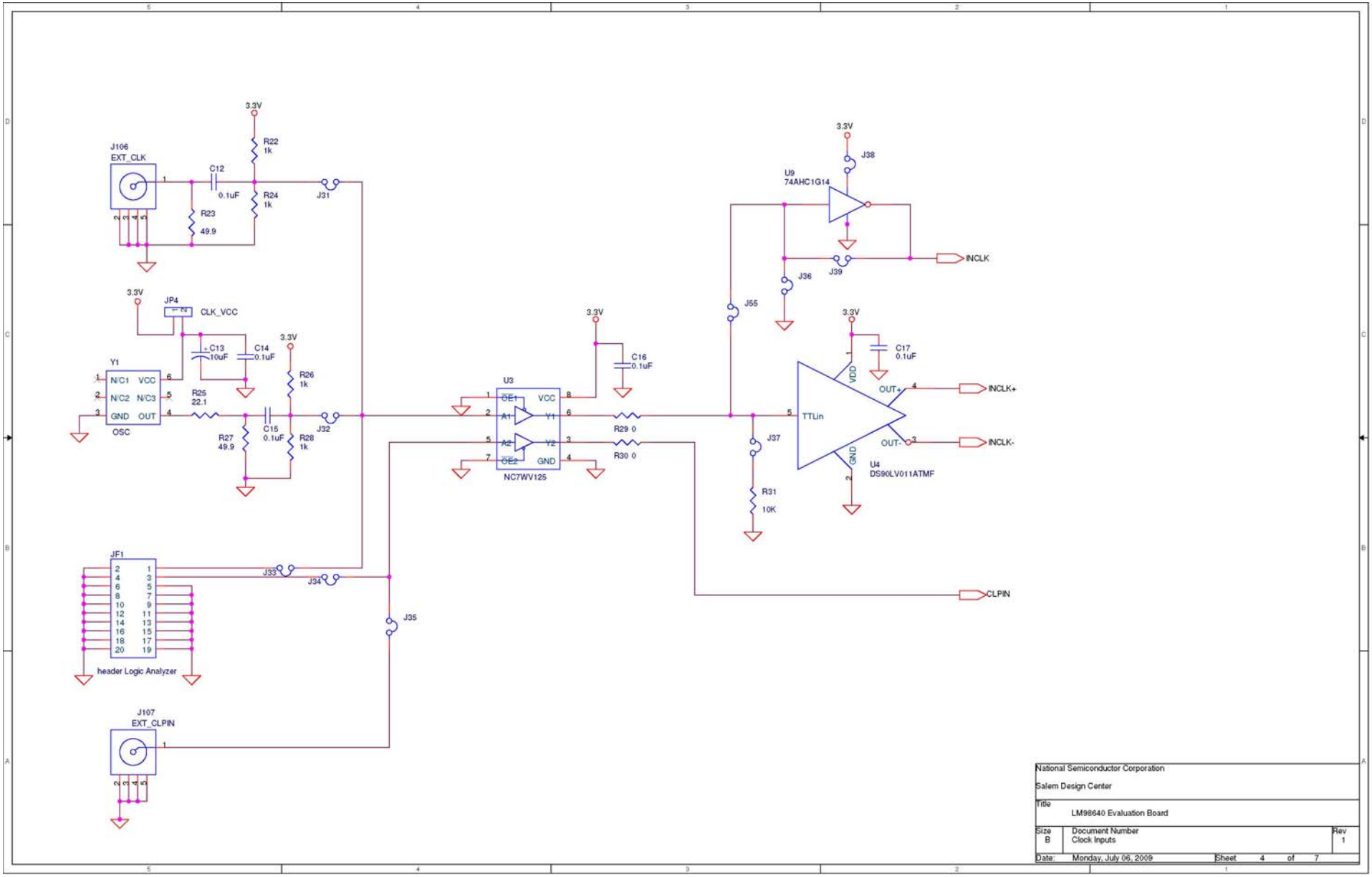
4.2 Page 2: Analog Front End Section



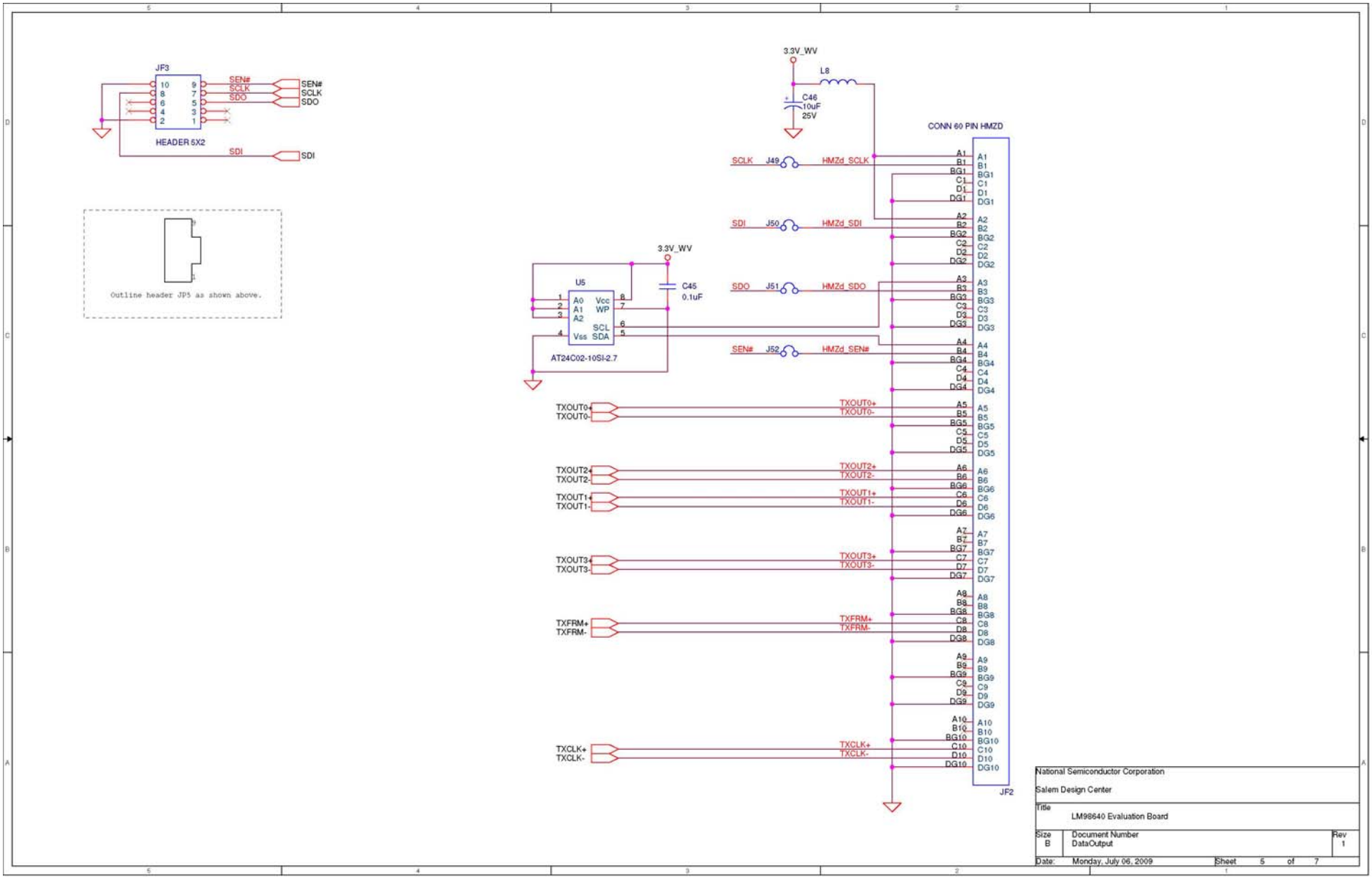
4.3 Page 3: Analog Input Section



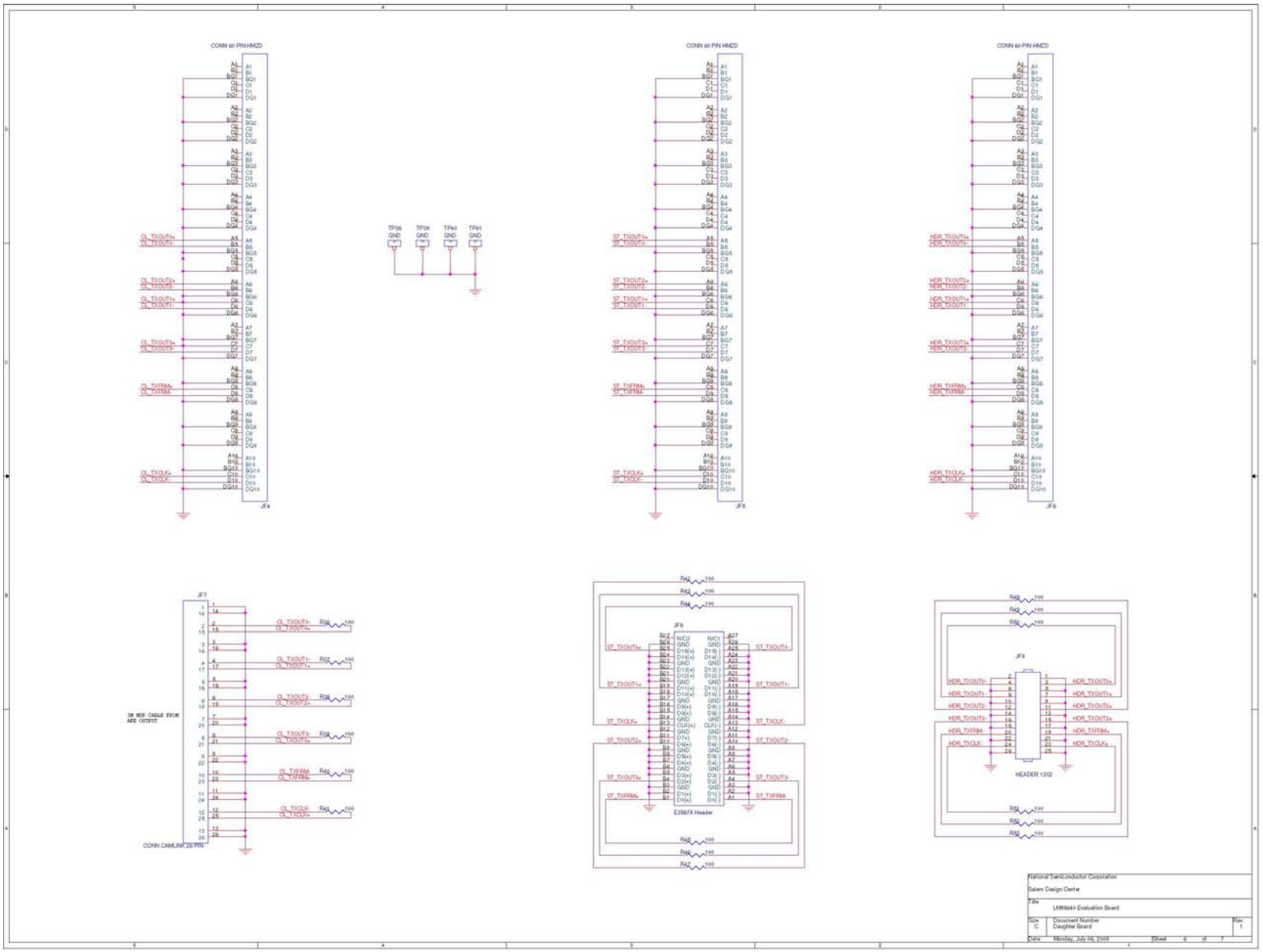
4.4 Page 4: Clock Input Section



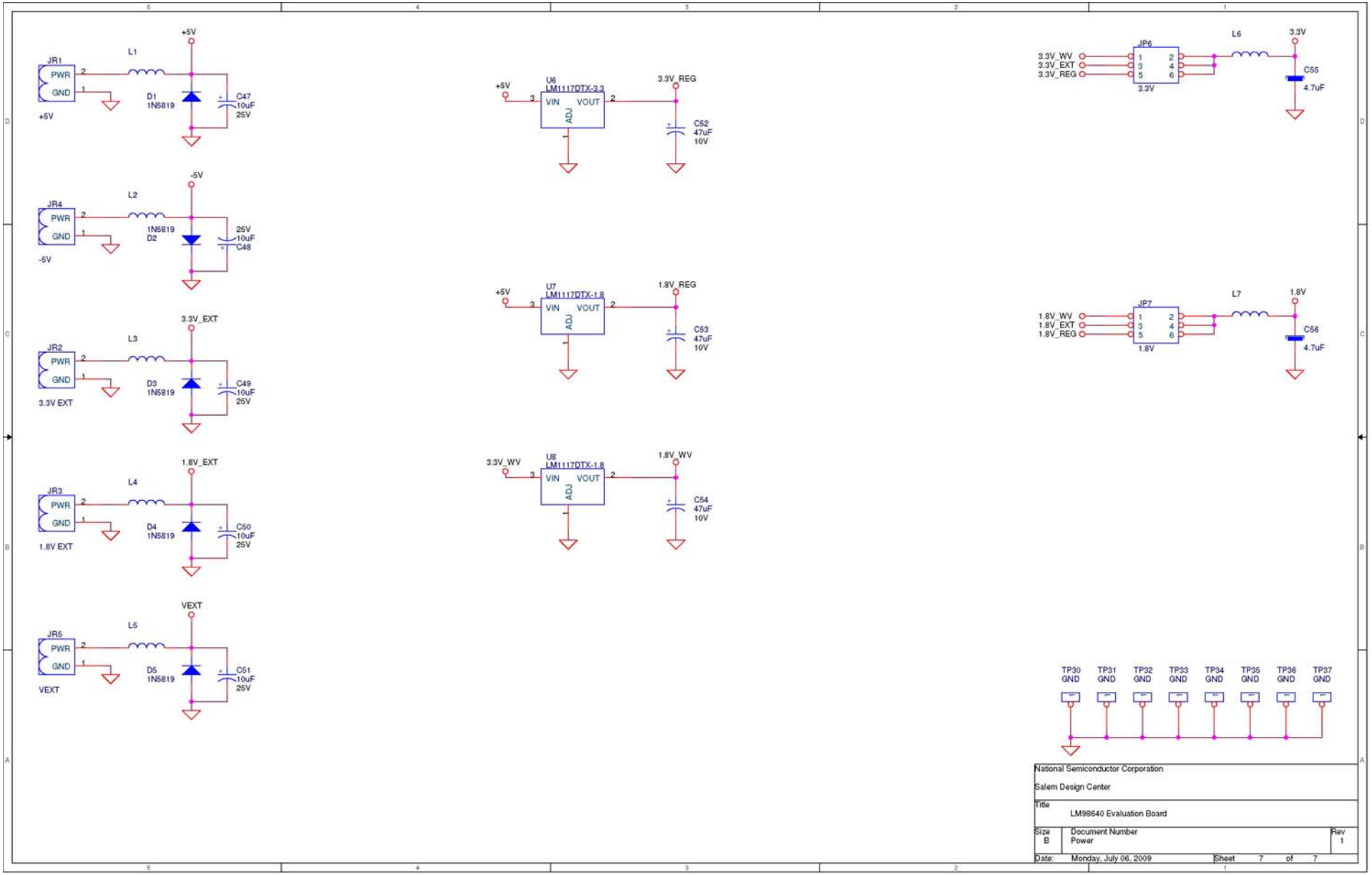
4.5 Page 5: Data Output Section



4.6 Page 6: Daughter Board Connector



4.7 Page 7: Power Input Section



5.0 Evaluation Board Specifications

Main Board Size:	3.75in x 5in
Daughter Board Size	1.25in x 5in
Clock Frequency Range :	5 MHz to 40 MHz
VEXT Input Voltage Range	0 to 18V
+5V EXT Input Voltage Range	5.0V +/- 10%
-5.0V EXT Input Voltage Range	-5.0V +/- 10%
+3.3V EXT Input Voltage Range	3.3V +/- 10%
+1.8V EXT Input Voltage Range	1.8V +/- 10%

6.0 Bill of Materials

Item	Quantity	Reference	Part	Part Number
1	4	C1,C2,C4,C5	0.1uF	PCC1828CT
2	2	C3,C6	300pF	490-1362-1-ND
3	7	C7,C12,C14,C15,C16,C17,	0.1uF	PCC1762CT
		C45		
4	24	C8,C10,C18,C20,C22,C23,	0.1uF	PCC2146CT
		C24,C25,C26,C27,C28,C29,		
		C30,C31,C32,C33,C35,C36,		
		C37,C38,C39,C40,C41,C42		
5	2	C9,C11	0.01uF	PCC103BQCT
6	1	C13	10uF	399-3683
7	2	C19,C21	1uF	PCC2364CT
8	1	C34	4.7uF	PCC1842CT
9	2	C43,C44	DNP	
10	6	C46,C47,C48,C49,C50,C51	10uF	478-3289-1
11	3	C52,C53,C54	47uF	478-3264-1
12	2	C55,C56	4.7uF	399-3699-1
13	5	D1,D2,D3,D4,D5	1N5819	B140-FDICT
14	1	JF1	header Logic Analyzer	S2011E-10
15	1	JF2	CONN 60 PIN HMZD	6469028-1
16	1	JF3	HEADER 5X2	S2011E-5
17	3	JF4,JF5,JF6	CONN 60 PIN HMZD	6469169-1
18	1	JF7	CONN CAMLINK 26 PIN	3M1819
19	1	JF8	E3587A Header	E5387-68701
20	1	JF9	HEADER 13X2	S2011E-13
21	1	JP1	SHUTDOWN	S1011E-2
22	1	JP4	CLK_VCC	S1011E-2
23	1	JP6	3.3V	S2011E-3
24	1	JP7	1.8V	S2011E-3
25	1	JR1	+5V	277-1150
26	1	JR2	3.3V EXT	277-1150
27	1	JR3	1.8V EXT	277-1150
28	1	JR4	-5V	277-1150
29	1	JR5	VEXT	277-1150
30	55	J1,J2,J3,J4,J5,J6,J7,J8,	jumper/sm/small	N/A
		J9,J10,J11,J12,J13,J14,		
		J15,J16,J17,J18,J19,J20,		
		J21,J22,J23,J24,J25,J26,		
		J27,J28,J29,J30,J31,J32,		
		J33,J34,J35,J36,J37,J38,		
		J39,J40,J41,J42,J43,J44,		
		J45,J46,J47,J48,J49,J50,		
		J51,J52,J53,J54,J55		
31	1	J101	OS1-	J500-ND
32	1	J102	OS1+	J500-ND

33	1	J103	VCLP	J500-ND
34	1	J104	OS2-	J500-ND
35	1	J105	OS2+	J500-ND
36	1	J106	EXT_CLK	J500
37	1	J107	EXT_CLPIN	J500
38	7	L1,L2,L3,L4,L5,L6,L7	10nH	490-1055-1
39	1	L8	10nH	BLM31PG500SN1L
40	2	Q1,Q2	MMBT3904/SOT	MMBT3904-FDICT
41	8	R1,R2,R7,R8,R16,R17,R34,	49.9	P49.9LCT
		R35		
42	4	R3,R4,R9,R10	150	P150CCT
43	2	R5,R11	0	311-0.0ARCT
44	2	R6,R12	1.5k	P1.5KACT
45	5	R13,R22,R24,R26,R28	1k	P1.00KHCT
46	2	R14,R15	75	P75.0HCT
47	4	R18,R19,R20,R21	20k	P20.0KHCT
48	2	R23,R27	49.9	P49.9HCT
49	1	R25	22.1	P22.1HCT
50	2	R29,R30	0	311-0.0GRCT
51	2	R31,R33	10k	P10.0KHCT
52	19	R32,R36,R37,R38,R39,R40,	100	P100LCT
		R41,R42,R43,R44,R45,R46,		
		R47,R48,R49,R50,R51,R52,		
		R53		
53	1	TP1	OS1-	S1011E-1
54	1	TP2	OS1+	S1011E-1
55	1	TP3	OS2+	S1011E-1
56	1	TP4	OS2-	S1011E-1
57	1	TP5	VCLP	5015KCT
58	1	TP6	VREFT2	5015KCT
59	1	TP7	VREFB2	5015KCT
60	1	TP8	VCOM2	5015KCT
61	1	TP9	VCOM1	5015KCT
62	1	TP10	VREFB1	5015KCT
63	1	TP11	VREFT1	5015KCT
64	1	TP12	ATB1	5015KCT
65	1	TP13	ATB0	5015KCT
66	10	TP14,TP17,TP18,TP19,TP20,	GND	S1011E-1
		TP21,TP38,TP39,TP40,TP41		
67	1	TP15	DTM0	S1011E-1
68	1	TP16	DTM1	S1011E-1
69	1	TP22	INCLK-	5015KCT
70	1	TP23	INCLK+	5015KCT
71	8	TP30,TP31,TP32,TP33,TP34,	GND	5015KCT
		TP35,TP36,TP37		
72	1	U1	LM98640QML	LM9864W-MPR
73	1	U2	LMH6572	LMH6572MQ

74	1	U3	NC7WV125	NC7WV125K8X
75	1	U4	DS90LV011ATMF	DS90LV011ATMF
76	1	U5	AT24C02-10SI-2.7	511-M24C02-WMN6P
77	1	U6	LM1117DTX-3.3	LM1117DTX-3.3
78	2	U7,U8	LM1117DTX-1.8	LM1117DTX-1.8
79	1	U9	74AHC1G14	296-1092-1-ND
80	1	Y1	OSC	N/A

7.0 Appendix A: Using the AFEval software and the Wavevision 5 Data Capture Board

IMPORTANT NOTE: Before connecting this board to the PC, please install the AFEval Software from the CDROM included with the development kit or file provided by your National Semiconductor representative. (See Appendix C)

Connecting the Development Board before installation may result in the board being registered as an unknown USB device. If this happens you will need to uninstall the device using the Windows Device Manager before installing the AFEval Software.

7.1 Connecting the WV5 board and LM98640CVAL board for the first time

This development board is designed to connect to a National Semiconductor Wavevision 5 Data Capture Board (WV5) through the HMZD connector JF2 and connect to a PC over a USB interface running the AFEval Software. The WV5 board comes with its own software GUI. This Wavevision 5 Software is typically used with National Semiconductor's High Speed ADC devices and is not required for use with the LM98640CVAL board.

1. With all power off, and the USB cable disconnected, connect the Wavevision 5 board (connector U2) to the LM98640CVAL board (connector JF2).
2. Configure the JP6 and JP7 jumpers on the LM98640CVAL board for the desired power supply source. For initial experiments, it is recommended that the jumpers are configured between pins 1 and 2 to allow supply power from the WV5 board.
3. Plug in the AC-DC power supply to the J2 connector on the Wavevision 5 board. Turn the red rocker switch to the On position and confirm that the Green LED is illuminated.
4. Connect the USB cable from the PC to the Wavevision 5 board.
5. Allow time for the PC to detect the WV5 board and load the appropriate drivers.

7.2 Proper Board Connection and Power Sequencing

The LM98640QML board should remain connected to the WV5 board unless modifications are required. To connect or disconnect the LM98640QML board from the system, the following sequences should be observed. Hot swapping of the LM98640CVAL board to WV5 is not recommended.

Connection Sequence:

1. AFEval software should be closed.
2. All power supplies are off.
3. USB connection to the WV5 board is disabled.
4. Enable the power supply to the WV5 board.
5. Enable the external power supplies to the LM98640CVAL board.
6. Connect the USB cable to the WV5 board.
7. Start the AFEval software.

Disconnection Sequence

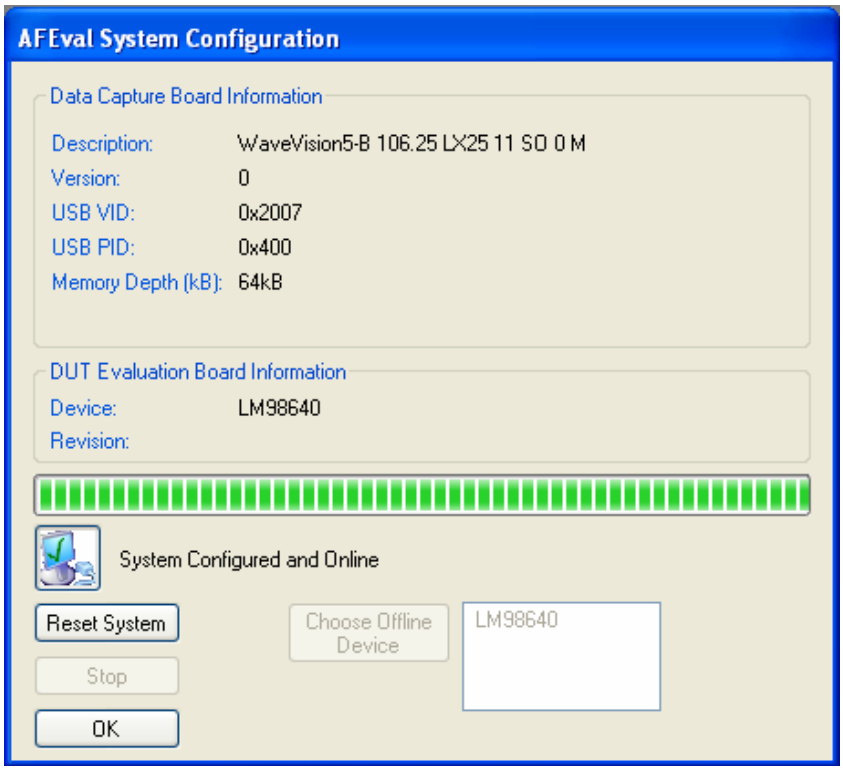
1. Close the AFEval software.
2. Disconnect the USB cable from WV5.
3. Disable any external power supplies feeding the LM98640CVAL board.
4. Turn the WV5 power switch to the Off position.

7.3 Starting the AFEval software

Start the AFEval software (Start -> All Programs -> National Semiconductor -> AFEval)

The software may take a few seconds to initialize, but should display an “About” screen similar to the following.

Following the “About” screen, the software will attempt to communicate to the WV5 board.



Once the WV5 board has been detected and configured, the software will search for any connected DUT Board and its associated software file (dll). If the LM98640CVAL is detected, the software will load the device’s software file, the proper FPGA image and then the LM98640QML Evaluation Environment.

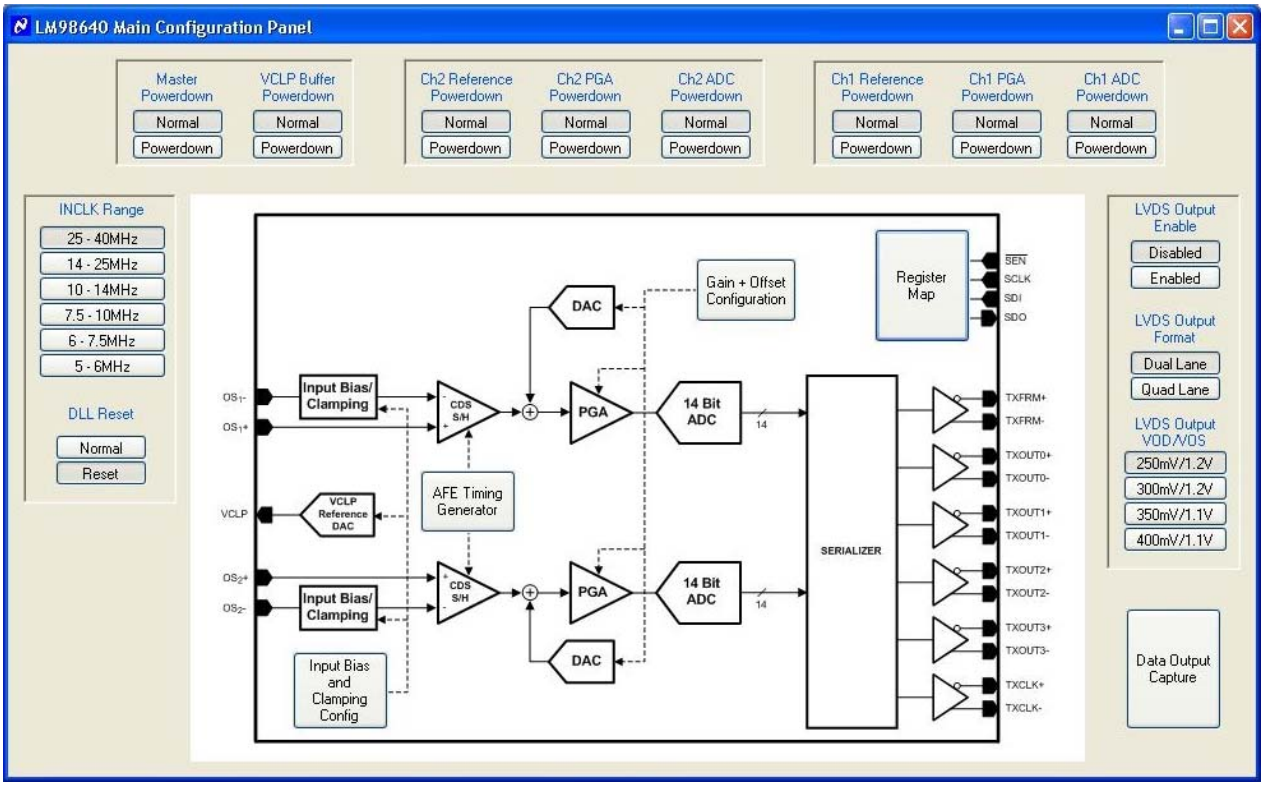
If the System Configuration does not succeed in finding the WV5 board or the LM98640CVAL Evaluation Board, the “Choose Offline Device” Option will be available. The list box next to the Choose Offline Device Button will list all available device software files (dlls) that are present on the installed PC. To configure the AFEval software environment to work without WV5 hardware communication, select one of the available devices in the list box, and then hit the “Choose Offline Device” button. If the software finds a valid AFE definition file for the device, it will open the evaluation environment for the requested device. Device dll files are located in the same directory as the installed executable file. Definition files are located in the directory **<install directory>\def**, where **<install directory>** is the path to the AFEval executable after installation. The “**\def**” directory contains device specific register definition files in an XML formatted document.”

If the WV5 board has not been detected, check that the USB drivers are installed correctly, then disconnect and re-connect the USB cable. If all connections and the external power supplies have been verified, hit the “Reset System” button in the System Configuration Window to start the configuration. If the WV5 board still fails to be detected, depress the SW2 reset button on the WV5 board and restart the AFEval software.

If the WV5 board is detected properly, but the LM98640CVAL board has not, verify that the HMZD connector is seated in properly and that the power supplies are configured properly.

7.4 LM98640QML Main Configuration Panel

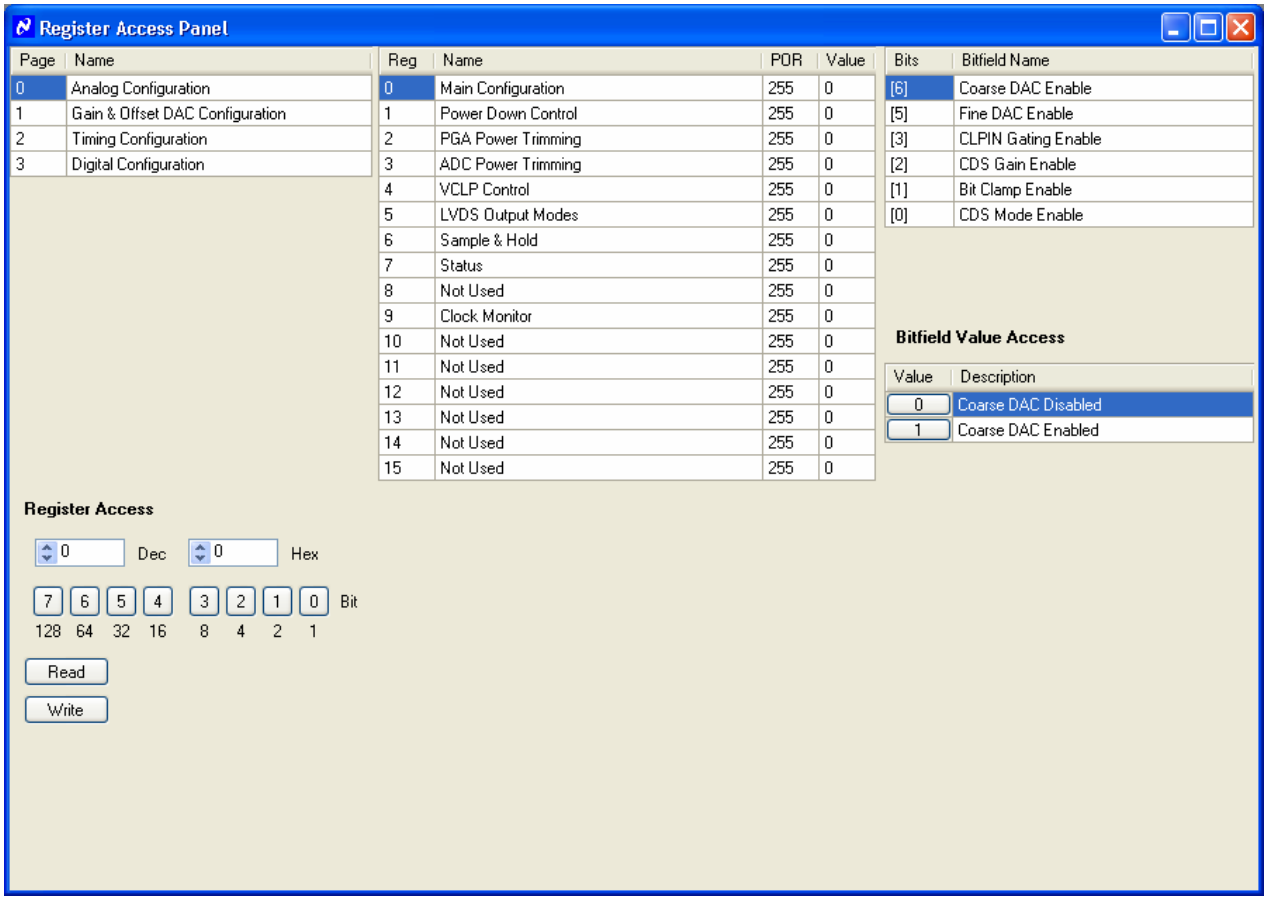
Once the FPGA Firmware download has completed and the LM98640CVAL is recognized, the software will load the LM98640QML Evaluation Environment. The Main Configuration Panel will be automatically displayed as shown.



The Main Configuration Panel gives a top level view of the LM98640QML. The system clocking settings of the device is configured using the controls on the left edge of the window. The Powerdown features of the device are configured using the controls on the top edges of the window. LVDS Output features are configured using the controls of the right edge of the window. In the center is a block diagram with buttons that will open other windows allowing a GUI assisted configuration of the device.

7.5 Register Access Panel

When the Register Map Button is selected, the register access panel will be displayed. This access panel allows bit level modification to any of the LM98640QML's configuration registers.



Using the Register Access panel is a simple way to modify individual bits, groups of bits, or entire registers at once. To access a different register page in the LM98640QML, click on the "Page" data grid on the upper right part of the form. The contents of that page will be shown in the "Register" level data grid filling the center of the window. Clicking on individual registers in the "Register' data grid will expose the register's Bitfield names in the Bitfield data grid on the right side of the window.

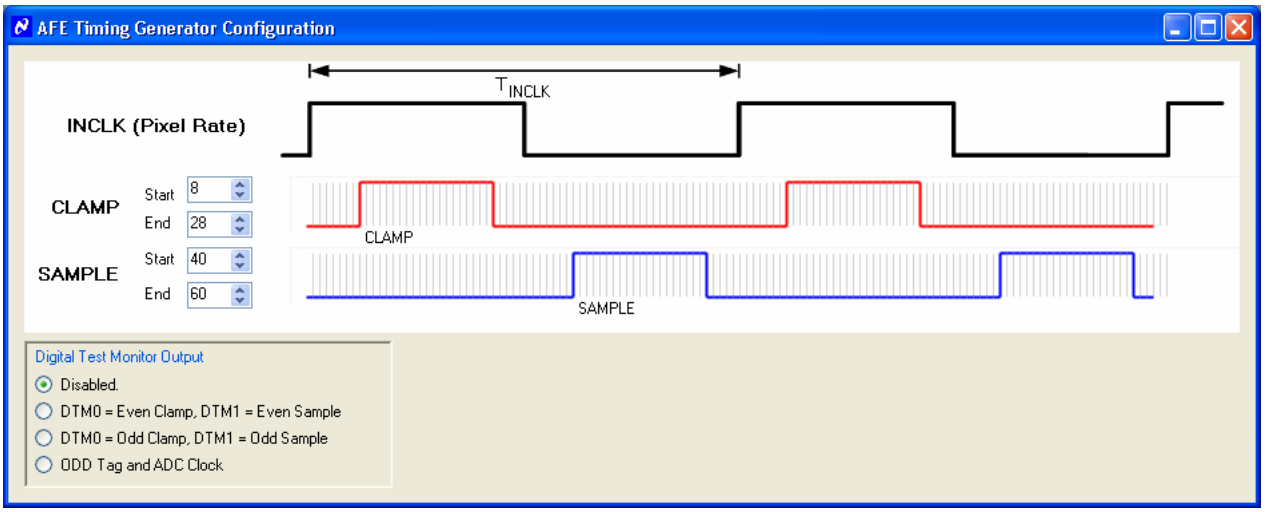
You can modify the selected register's contents by clicking on the individual bit buttons (shown above the "Read" and "Write" buttons), or by modifying the decimal or hexadecimal text box contents. The "Value" data grid can also be used to modify the selected Bitfield of the chosen register. The "Value" data grid will show bit level buttons for discrete value types (as seen in the diagram above), or a slider control for continuous value types such as DAC values or PGA values.

If the Wavevision 5 Data Capture hardware is configured properly, any change to the LM98640QML register set will be automatically written to the device through the SPI. To confirm this operation, pressing the "Read" button, will perform an SPI read of the currently selected register map page.

Please refer to the LM98640QML datasheet for a full description of the AFE's internal registers.

7.6 AFE Timing Generator Window

The LM98640QML AFE Timing Generator settings can be programmed with the aid of the window shown below.



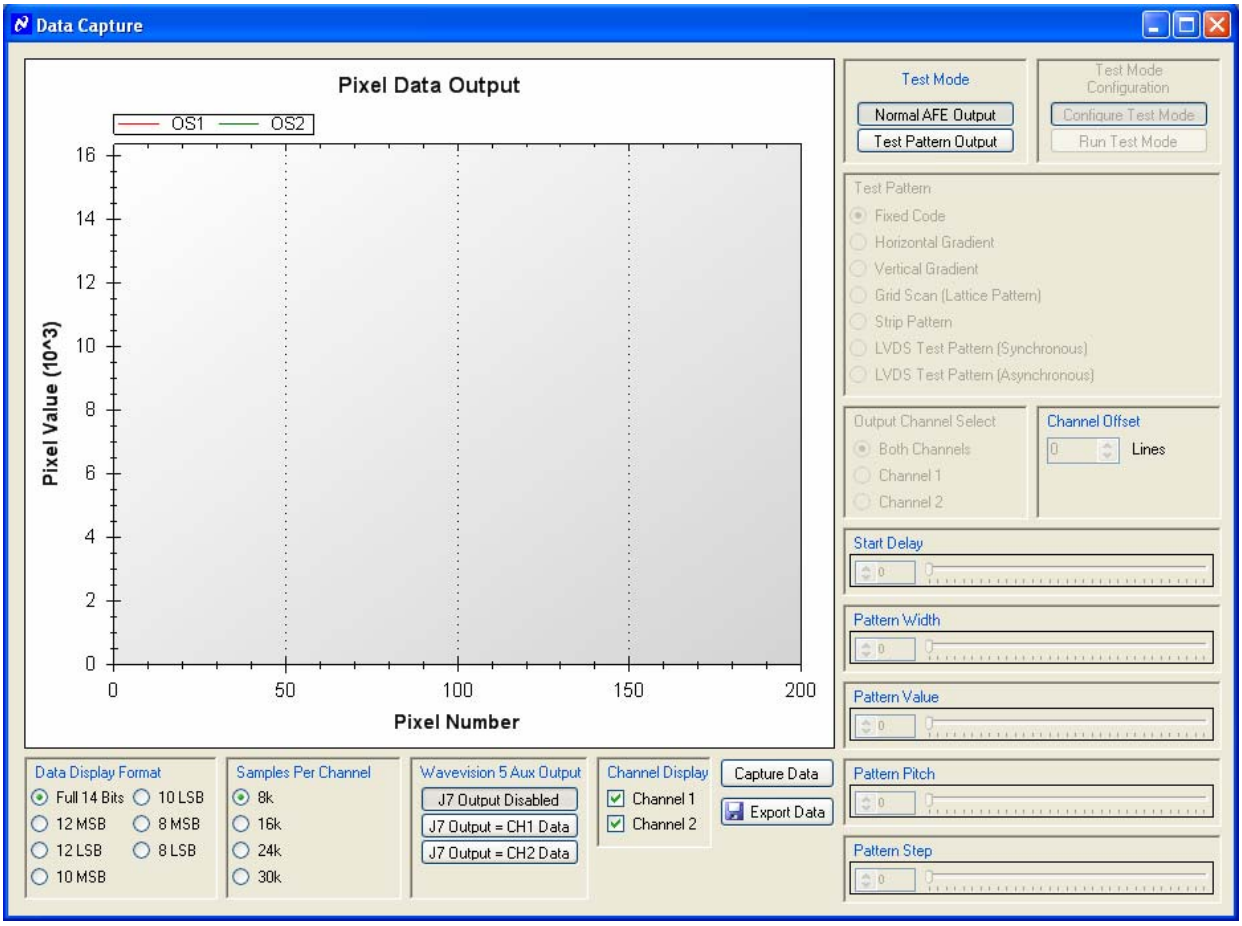
The AFE Timing Generator is used to align the CLAMP and SAMPLE pulses over the appropriate portions of the input signal. First, the user should enable the Digital Test Monitor pins by selecting one of the radio buttons in the lower left control. The user can than monitor the CLAMP and SAMPLE pulses along with the input signal on a scope and use the Start/End numeric controls to align the pulses to their appropriate positions. The text under each waveform identifies which clamp and sample pulses are related.

In Sample & Hold mode the CLAMP and SAMPLE pulses occur at the same time, and the CLAMP values are disabled. Also note that in Sample & Hold mode only the Odd Clamp and Odd Sample pulses can be selected as a Digital Test Monitor Output selection.

7.7 AFEval Data Display

When used in conjunction with the Wavevision 5 Data Capture Board, the AFEval software is able to capture and display the LVDS data output from the LM98640QML.

To open the display window choose the “Tools” item on the main window’s menu bar. Select the “Data Capture…” item. The display should appear similar to the window below.



The Data Acquisition depth can be adjusted from 8k samples to 30k samples.

To collect the AFE’s output data from the actual ADC conversions, depress the “Normal AFE Output” button. Subsequent data captures will be the AFE output.

To test the data path itself, several LM98640QML Test Patterns can be chosen. Refer to the datasheet for more information on the available test patterns and how to properly configure the selected pattern.

To Zoom In on the waveform:

1. Depress the left mouse button (keeping it down) and drag the mouse to select the desired window width.
2. Lift the left mouse button when you have reached the end of the desired zoom window.

To Zoom Out on the waveform:

1. Simply right click over the waveform and select the menu item “Un Zoom” or Undo All Zoom/Pan”.

To Pan on the waveform:

1. While depressing the Ctrl key, depress the left mouse button (keeping it down) and drag the mouse to move the waveforms position in the window.
2. Lift the left mouse button when you have reached the desired position.

To Un-Pan on the waveform:

Simply right click over the waveform and select the menu item “Un Pan” or Undo All Zoom/Pan”.

8.0 Appendix B: Using the AFEval software and the Total Phase Aardvark SPI Interface

IMPORTANT NOTE: Before connecting this board to the PC, please install the AFEval Software from the CDROM included with the development kit or file provided by your National Semiconductor representative. (See Appendix C)

Connecting the Development Board before installation may result in the board being registered as an unknown USB device. If this happens you will need to uninstall the device using the Windows Device Manager before installing the AFEval Software.

While using the Total Phase Aardvark SPI device, the Wavevision 5 Data Capture board should not be connected.

8.1 Install the device drivers for the Aardvark device.

The drivers for the Aardvark SPI module should be installed according to the instructions and CD which accompanied the device.

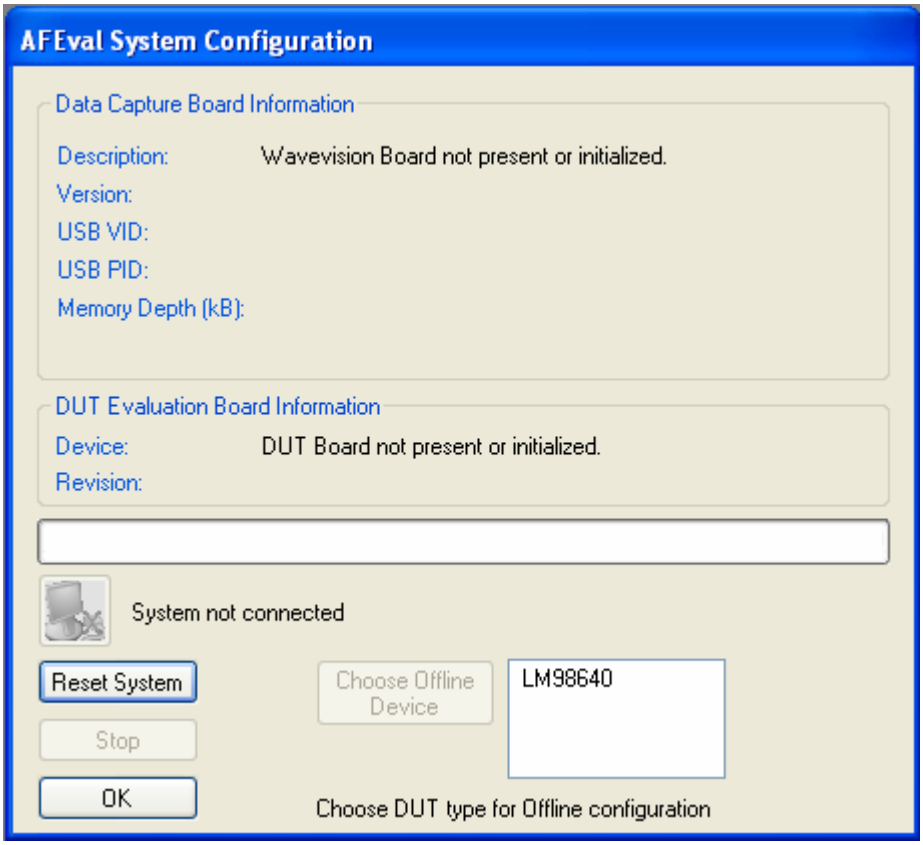
8.2 Connecting the Aardvark SPI device and LM98640CVAL board for the first time

To facilitate external test equipment based data capture, the LM98640CVAL development board allows for SPI communication through a 2x5 dual row header. The Total Phase Aardvark SPI device is supplied to provide this communication using the AFEval software.

1. With all power off, and the USB cable disconnected, connect the Aardvark device to the LM98640CVAL board (connector JF3).
2. Configure the JP6 and JP7 jumpers on the LM98640CVAL board for the desired power supply source. While using the external SPI (and not the WV5 board), the power for the LM98640CVAL board should be configured via pins 3-4 or 5-6 on the JP6 and JP7 connectors.
3. Connect the USB cable from the PC to the Aardvark device.
4. Allow time for the PC to detect the Aardvark board and load the appropriate drivers.
5. Start the AFEval software.

8.3 Aardvark SPI Communication via AFEval

The AFEval software will by default search for a connected Wavevision 5 Data capture board upon start-up. If no WV5 board is detected the software will show the following screen:



Using the mouse, click on the “LM98640” text in the list box, then click the “Choose Offline Device” button. The software will then search for the Aardvark device. If the Aardvark device is detected, it will become the source of SPI communication. The Data Capture GUI will still be available to aid in configuring the various test mode outputs, but the actual data capture will not be functional due to the absence of a WV5 board.

If the Aardvark device becomes disconnected from the USB port while running, the AFEval software will need to be restarted to establish proper communication.

9.0 Appendix C - Installing and running the AFEval software

9.1 Uninstall previous versions of AFEval Software.

- Open the Control Panel from the Windows Start Menu.
- Choose “Add or Remove Programs”.
- Choose to remove any previous version of the AFEval Software and any LM98640QML Plugin Module that exists on the system.

9.2 Install the AFEval Software.

- Insert the AFEval CD-ROM into your computer’s CD-ROM drive.
- The AFEval software uses the Microsoft® .NET technology. For detailed information on AFEval’s use of .NET technology, please see below. If your computer does not have this software, the AFEval installer will instruct you on how to install it.
- Locate and run the **AFEval_Setup.exe** program on the CD-ROM. Follow the on-screen instructions to finish the install.

9.3 Microsoft® .NET Framework

The AFEval software uses the Microsoft® .NET Framework. The underlying .NET Framework must be installed on your computer in order for the AFEval software to run. The software can run with .NET 2.0 or higher.

The AFEval installer will first look for an existing copy of the .NET Framework on your computer. If it is not found, the installer will ask if you want to install it. Follow the on-screen instructions to finish the install.

AFEval software contains Windows specific hardware interface code and therefore is only currently supported under Windows.

9.4 Windows Driver

The AFEval software communicates with the Wavevision 5 hardware through the Windows device driver software. If you are unable to connect to the Wavevision board after installing the software, do the following to uninstall and reinstall the driver. Go to the Windows Control Panel and select System. If you are using Windows 2000/XP select the Hardware tab. Then click on Device Manager and go down to the Universal Serial Bus controllers. With the Wavevision 5 board connected, you will see it (or an unknown device) listed. Right click on it and uninstall the driver. Then unplug and plug in the board again to reinstall the driver.

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